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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 29/06, 29/24, 21/04, 29/872 — A1

(11) International Publication Number: **WO 97/27629**

(43) International Publication Date: 31 July 1997 (31.07.97)

(21) International Application Number: PCT/US97/00335

(22) International Filing Date: 13 January 1997 (13.01.97)

(30) Priority Data:
08/590,782 24 January 1996 (24.01.96) US

(60) Parent Application or Grant
(63) Related by Continuation
US 08/590,782 (CON)
Filed on 24 January 1996 (24.01.96)

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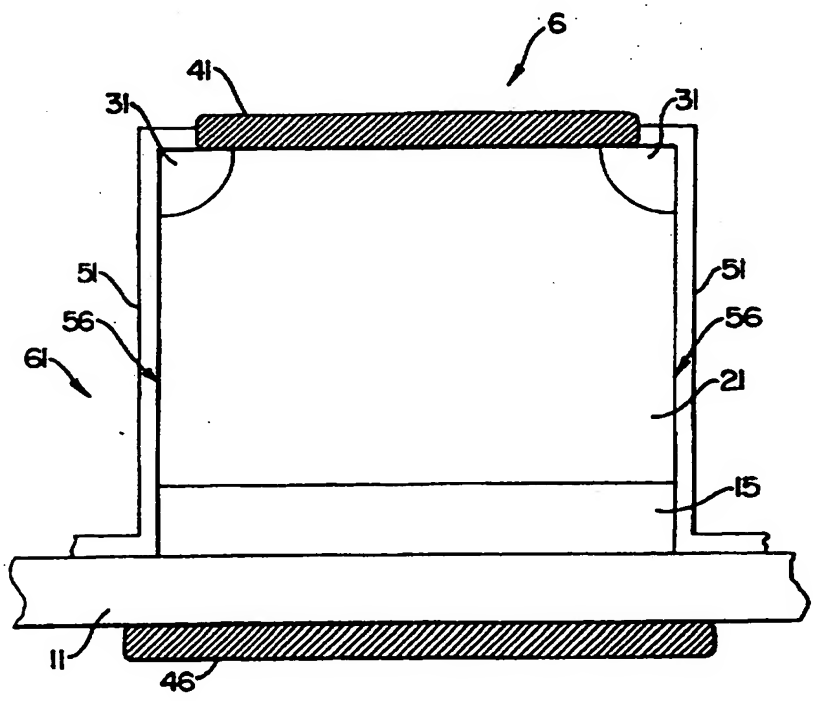
(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: MESA SCHOTTKY DIODE WITH GUARD RING

(57) Abstract

A Schottky barrier diode (5) comprises a bulk single crystal semiconductor material substrate (10), an optional first epitaxial layer (15) of n-type conductivity semiconductor material formed upon the substrate, and a second epitaxial layer (21) of n-type conductivity semiconductor material formed upon the first epitaxial layer. The second epitaxial layer has formed on it a Schottky contact (41) having the periphery of which is defined by the edges of the Schottky contact. The second epitaxial layer has formed in it regions (31) of p-type conductivity semiconductor material formed wherein the regions (31) are formed about the periphery of the Schottky contact (41). The diode also has an ohmic contact (46) formed on the substrate opposite the epitaxial layers. The epitaxial layers of the diode form a mesa having sidewalls (56) which define the periphery of the diode and extend downward through the regions (31) of p-type conductivity semiconductor material and the epitaxial layer (15, 21). A method of reducing leakage current and increasing breakdown voltage in a Schottky barrier diode by forming p-type regions about the periphery of the Schottky contact etching through the p-type regions to form a mesa.



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MESA SCHOTTKY DIODE WITH GUARD RING.

Field of the Invention

The present invention relates to Schottky barrier diodes and more particularly to Schottky barrier diodes formed in silicon carbide.

Background of the Invention

As demands for higher speed, higher power devices increases, the need for diodes having faster switching speeds and increased reverse bias breakdown voltages has also increased. Applications such as power modules for motor and generator control, electronic ballasts for lighting control, industrial robots, display drivers, automotive ignition and automation control would all benefit from higher power, higher speed diodes. Unfortunately, existing implementations of higher speed Schottky barrier diodes or P-i-N diodes have had limited success in creating diodes with a high reverse bias breakdown voltage, a low leakage current and a low forward on-state resistance.

One such device which attempted to raise the reverse bias breakdown voltage is the Junction Barrier controlled Schottky (JBS) rectifier. The JBS rectifier is a Schottky rectifier having an array of Schottky contacts at the face of a semiconductor substrate with corresponding semiconductor channel regions beneath the contacts. The JBS rectifier also includes a P-N junction grid interspersed between the Schottky contacts. This device is also referred to as a "pinch" rectifier, based on the operation of the P-N junction grid. The P-N junction grid is designed so that the depletion layers extending from the grid into the substrate will not pinch-off the channel regions to

forward-biased currents, but will pinch-off the channel regions to reverse-biased leakage currents.

Under reverse bias conditions, the depletion layers formed at the P-N junctions spread into the channel regions, beneath the Schottky barrier contacts. The dimensions of the grid and doping levels of the p-type regions are designed so that the depletion layers intersect under the array of Schottky contacts, when the reverse bias exceeds a few volts, and cause pinch-off. Pinch-off of the channels by the depletion layers causes the formation of a potential barrier in the substrate and further increases in the reverse-biased voltage are supported by the depletion layer, which then extends into the substrate, away from the Schottky barrier contacts. Accordingly, once a threshold reverse-biased voltage is achieved, the depletion layers shield the Schottky barrier contacts from further increases in reverse-biased voltage. This shielding effect prevents the lowering of the Schottky barrier potential at the interface between the metal contacts and semiconductor substrate and inhibits the formation of large reverse leakage currents.

The design and operation of the JBS rectifier is described in Section 8.4 of *Modern Power Devices* by Baliga and in U.S. Patent No. 4,641,174. Unfortunately, the JBS rectifier typically possesses a relatively large series resistance and a relatively large forward voltage drop caused by the reduction in overall Schottky contact area dedicated to forward conduction. This reduction in area is necessarily caused by the presence of the P-N junction grid at the face of the substrate. In addition, large forward currents can cause large forward voltage drops and can lead to the onset of minority carrier conduction (i.e., bipolar), which limit the JBS's performance at high switching rates.

Other devices have reported reductions in on-state resistance but have not resulted in high reverse bias breakdown voltages. See for example, U.S. Patent No. 5,365,102. These efforts have also required increased area for fabrication of the diode device.

Efforts have also been directed at improving diode performance through the use of alternative semiconductor materials such as silicon carbide. However, limitations in the design and fabrication of silicon carbide ("SiC") devices have resulted in the fabrication of SiC Schottky barrier diodes which exhibit less than predicted reverse bias characteristics. These devices have high reverse bias leakage currents and much lower reverse bias breakdown voltages than theoretically predicted for SiC devices. Furthermore, attempts to increase the breakdown voltage of Schottky devices require increased surface area over that used by the Schottky contact as these attempts were to spread out the electric field horizontally to reduce the field crowding occurring at the periphery of the Schottky contact. These attempts in the horizontal plane all required an increase in the surface area utilized by the diode device and thus reduced the yield of diodes per cm^2 of wafer area.

Therefore, there remains a need to develop high performance diodes which exhibit a high reverse bias breakdown voltage with low leakage currents. Also because of the physical properties of SiC there is also a need to develop structures and fabrication techniques which take advantage of the high thermal conductivity and other desirable properties to achieve the theoretical capabilities of SiC diodes. Furthermore, to maximize yield of a device which exhibits increased performance over traditional Schottky diode designs it would be desirable to provide such a device without increasing the area required for such a device.

Object and Summary of the Invention

Therefore, it is an object of the present invention to provide a semiconductor device structure for a Schottky barrier diode which can be fabricated in SiC and which takes advantage of the high thermal conductivity of SiC. It is also an object of the present invention to provide a Schottky barrier diode with high reverse bias blocking voltage and with low reverse bias leakage current. It is also an object of the present invention to provide a Schottky barrier contact diode with improved reverse bias and leakage current characteristics without requiring additional area to create such a device.

The present invention meets these objects with a Schottky barrier diode comprising a bulk single crystal substrate of n-type conductivity semiconductor material having a first surface and a second surface opposite the first surface. An epitaxial layer of n-type conductivity semiconductor material is formed on the first surface of the substrate. This epitaxial layer has a lower carrier concentration than that of the substrate. The diode according to the present invention also includes an ohmic contact formed on the second surface of the substrate opposite the epitaxial layer to provide a cathode contact. A Schottky contact is formed on the epitaxial layer to provide an anode contact. The Schottky contact has a periphery which is defined by the edges of the Schottky contact. The diode also includes regions of p-type conductivity semiconductor material formed in the epitaxial layer. These p-type regions are formed about the periphery of the Schottky contact and extend beneath the Schottky contact and past the edges of the Schottky contact. Between the p-type regions at the periphery of the Schottky contact there remains a region of contact between the n-type semiconductor material of the epitaxial layer and the Schottky contact.

Additionally, the substrate and the epitaxial layer of the diode of the present invention form a mesa having sidewalls which define the periphery of the diode. The sidewalls of the mesa extend downward through the regions of p-type conductivity and the epitaxial layer to the substrate. The diode of the present invention is preferably made of silicon carbide.

Optionally, the diode of the present may include an additional layer of n-type conductivity semiconductor material between the substrate and the epitaxial layer on which the Schottky contact is formed to provide first and second epitaxial layers respectively. This optional first epitaxial layer has a higher carrier concentration than the second epitaxial layer. The diode of the present invention may also include an insulating layer formed on the sidewalls of the mesa.

The present invention also provides a method of reducing the leakage current and increasing the breakdown voltage of a Schottky barrier diode having a Schottky contact formed on a lightly doped n-type conductivity epitaxial layer of semiconductor material. The method includes forming p-type conductivity regions in the n-type epitaxial layer of the Schottky barrier diode at the periphery of the Schottky contact of the diode. The diode is then etched through the p-type conductivity region and through the n-type conductivity epitaxial layer to form a mesa.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of a first embodiment of the present invention; and

Figure 2 is a cross-sectional view of a second embodiment of the present invention.

Detailed Description

The present invention provides a method and structure for increasing the breakdown voltage and

decreasing the leakage current of reverse biased Schottky barrier diodes. The present invention decreases the edge effects and field crowding present in previous Schottky barrier diodes and thus provides a Schottky barrier diode with increased breakdown voltage and decreased leakage current. The present invention provides a vertical Schottky contact diode having an n^- epitaxial layer with heavily doped p-type conductivity regions at the periphery of the Schottky contact. The periphery of the diode is then defined by forming a mesa which passes through the p^+ implanted region and through the n^- epitaxial layer.

Figure 1 illustrates one particular embodiment of the present invention. As seen in **Figure 1**, diode **5** includes a first epitaxial layer **20** formed on a bulk single crystal substrate **10**. The substrate **10** is preferably formed of n-type silicon carbide. The epitaxial layer **20** is also preferably formed of n-type silicon carbide. The n-type substrate **10** is preferably a heavily doped n^+ 4H silicon carbide substrate. The epitaxial layer **20** which is formed on the first surface of the substrate **10** is preferably a lightly doped n^- 4H silicon carbide layer. As used herein, "n^+" refers to regions that are defined by higher carrier concentration than are present in adjacent or other regions of the same or another epitaxial layer or substrate. Also, as used herein, "n^-" refers to regions that are defined by lower carrier concentration than are present in adjacent or other regions of the same or another epitaxial layer or substrate.

As is further illustrated in **Figure 1**, an ohmic contact **45** is formed on the surface of the substrate **10** opposite the surface on which the epitaxial layer **20** is formed. This ohmic contact may act as a cathode for the diode device. The diode **5** also includes a Schottky contact **40** formed on the surface of epitaxial layer **20** opposite substrate **10** .

This contact acts as an anode contact for the diode device. The Schottky contact **40** has a periphery which is defined by the edges of the Schottky contact.

Also, as shown in **Figure 1**, the diode **5** includes regions of p-type silicon carbide **30** formed at the periphery of the Schottky contact **40**. These p-type regions circumscribe the Schottky contact at its edges. As shown in **Figure 1**, the p-type regions **30** are formed about the periphery of the Schottky contact **40** and extend beneath the Schottky contact **40** and past the edges of the contact while maintaining a region of contact between the n^- layer **20** and the Schottky contact **40**. Preferably the distance these p-type regions extend beneath the Schottky contact is kept to a minimum to provide as large a channel area in the n-type material of epitaxial layer **20**.

The diode **5** is also formed in the shape of a mesa **60**. The mesa **60** has sidewalls **55** which extend through the p-type regions **30** of epitaxial layer **20** and extend downward to substrate **10**. Optionally, the sidewalls **55** of the mesa **60** may extend into substrate **10**. The sidewalls **55** of mesa **60** are preferably formed as close to the edge of Schottky contact **40** as possible while still passing through the p-type regions **30**. Thus, the sidewalls **55** of the mesa **60** which defines the periphery of the diode **5** have a face which includes an n-type epitaxial layer and a p-type region at its upper edge.

Figure 2 illustrates an additional embodiment of the present invention. As seen in **Figure 2**, the diode **6** is comprised of a bulk single crystal n-type silicon carbide substrate **11** having a first surface and a second surface opposite the first. A n-type epitaxial layer **15** is formed on the first surface of substrate **11**. In **Figure 2**, the n-type substrate **11** and the epitaxial layer **15** are preferably both heavily doped n-type silicon carbide. A second epitaxial layer

21 is formed on the first epitaxial layer 15. The second epitaxial layer 21 is preferably a lightly doped n^- 4H silicon carbide epitaxial layer. As with the device shown in **Figure 1**, the diode 6 of **Figure 2** also has a Schottky contact 41 formed on the upper surface of the n^- epitaxial layer 21. The diode 6 also has p^+ regions 31 formed in the epitaxial layer 21 at the periphery of the Schottky contact 41. The diode 6 of **Figure 2** is etched into a mesa 61 the sidewalls of which extend downward through the epitaxial layer 21 and into epitaxial layer 15. The sidewalls 56 of the mesa 61 are formed such that they pass through the p-type regions 31.

Referring now to both **Figure 1** and **Figure 2**, optionally, diode 5 or 6 may have an insulating layer 50 or 51 formed on the sidewalls 55 or 56 of the mesa 60 or 61. The insulating layers 50 or 51 may optionally extend to the upper surface of the p-type regions 30 or 31.

In forming the mesa 60 or 61, it is preferred that the sidewalls 55 or 56 of the mesa begin as close as possible to the outer periphery of the Schottky contact 40 or 41, while still extending downward through the p-type regions formed in the epitaxial layers 20 or 21. Furthermore, the distance the p-type regions 30 and 31 formed in epitaxial layers 20 and 21, respectively, extend beneath the Schottky contacts 40 and 41, respectively, should be minimized. In practice, the practical limitations will result in an overlap of the p-type regions with the Schottky contact of from about 0.5 to about 50 microns. Also, the sidewalls 55 or 56 of the mesa will begin from about 0.5 to about 50 microns past the outer periphery of the Schottky contact. The depth of the p-type region within the epitaxial layer may be as little as 1000 angstroms or as deep as 5 microns. Also shown in **Figure 2**, the mesa 61 may optionally be etched through

epitaxial layer **15** into substrate **11**, thus providing sidewalls **56** which extend downward through epitaxial layers **21** and **15** and into substrate **11**. In such a case, the insulating layer **51** may be formed to cover both epitaxial layers.

With respect to the shape of the sidewalls **55** or **56** of the mesa **60** or **61**, these sidewalls may be vertical and substantially perpendicular to the upper surface of the substrate **10** or **11**. These sidewalls may also have a retrograde shape wherein the sidewalls **55** or **56** intersect the upper surface of the substrate **10** or **11** at an acute angle such that the mesa **60** or **61** formed by the sidewalls **55** or **56** is narrower at the bottom than at the top. Finally, the sidewalls may also intersect the upper surface of the substrate **10** or **11** at an obtuse angle such that the mesa **60** or **61** formed by the sidewalls **55** or **56** is wider at the bottom than at the top. In such a case the bottom of the mesa formed should be substantially wider than the top.

In operation, when forward biased by application of a positive voltage to the anode Schottky contact **40** or **41** with respect to the cathode contact **45** or **46**, current flows from the anode contact through the epitaxial layer **20** with respect to the diode in **Figure 1** or the epitaxial layers **21** and **15** with respect to the diode in **Figure 2**. Current then flows through the substrate **10** or **11** and to the cathode contact **45** or **46**. At very higher forward voltages, the application of a forward bias to the structure of the present invention creates both the forward biased Schottky barrier and a forward biased P-N junction which results from the p-type implanted regions **30** or **31**.

When reverse biased by application of a negative voltage to the anode Schottky contact **40** or **41** with respect to the cathode contact **45** or **46** no current should flow from the anode contact through the epitaxial layer **20** with respect to the diode in **Figure**

1 or the epitaxial layers 21 and 15 with respect to the diode in **Figure 2** and no current should flow through the substrate 10 or 11 and to the cathode contact 45 or 46. The application of a reverse bias to the structure of the present invention also creates a reverse biased P-N junction at the periphery of the Schottky contact which is less susceptible to edge effects than Schottky barriers and when combined with the mesa structure would prevent the electric field crowding to thereby reduce leakage current and increase breakdown voltage.

In fabricating devices according to one embodiment of the present invention, the lightly doped n silicon carbide layers are epitaxially grown on a heavily doped n^+ silicon carbide substrate. The doping and thickness of the n^- epitaxial layer is dependent upon the designed breakdown voltage of the device.

In forward bias, where the anode of the device is at a positive voltage with respect to the cathode, the current density (J) through the device may be approximately predicted using the following equation:

$$J = A^* T^2 e^{\frac{-(q\,\phi_B)}{kT}} e^{\frac{qV}{kT}}$$

where A^* is the Richardson Constant which is about 110 Amps/cm^{2}K^2 for 4H SiC, ϕ_B is the metal-semiconductor barrier height, q is the electron charge, V is the applied voltage, k is Boltzmann's Constant and T is the temperature in Kelvin.

The leakage current density (J_L) for the device in reverse bias (when a negative voltage is applied to the anode with respect to the cathode) is approximately predicted by the following equation:

$$J_L = A^* T^2 e^{\frac{-(q\phi_{Bn})}{kT}}$$

where ϕ_{Bn} is given by $\phi_B - \Delta\phi_B$ where $\Delta\phi_B$ is given by the following equation:

$$\Delta\phi_B = \sqrt{\frac{qE}{4\pi\sigma_S}}$$

where E is the electric field at the metal-SiC junction and σ_S is the permitivity of SiC which is 8.854×10^{-13} farads/cm.

The breakdown voltage (BV) may be approximately predicted for 4H-SiC (assuming that W, the width of the n epitaxial layer is greater than $1.3 \times 10^{11} N_D^{-7/8}$) using the following equation:

$$BV = 1.58X10^{15} N_D^{-3/4} - V_{bi} - \frac{kT}{q}$$

where N_D is the doping of the N^- SiC epitaxial layer and V_{bi} is the built in voltage of the SiC Schottky barrier diode. V_{bi} may be determined using the following equation:

$$V_{bi} = \phi_M - (\chi_s + E_C - E_F)$$

where ϕ_M is the work function of the metal used to form the Schottky contact, χ_S is the electron affinity of SiC which is about 3.7 electron volts, E_C is the conduction band edge and E_F is the Fermi level for SiC. Furthermore the difference $E_C - E_F$ may be determined by the following equation:

$$E_C - E_F = \frac{E_G}{2} + \frac{KT}{q}\ln\left(\frac{N_D}{n_j}\right)$$

where E_G is the bandgap of SiC (about 2.36 for 4H SiC), K is Boltzmann's constant, T is the temperature, q is

the electron charge ($1.6 \times 10^{-19}C$), N_D is the doping of the SiC at the metal-semiconductor junction and n_i is the intrinsic carrier concentration of SiC which is about 2.3×10^{-15} cm^{-3} at room temperature.

In each of the embodiments described above, the substrate is preferably formed of silicon carbide selected from the group of 2H, 6H, 4H, 15R or 3C silicon carbide and the epitaxial layers are formed of silicon carbide selected from the group of 2H, 6H, 4H, 15R or 3C silicon carbide. As described above, most preferably the substrate and the epitaxial layers are formed of 4H silicon carbide.

With respect to the p-type regions **30** and **31**, these regions should be as heavily doped as possible without causing excessive fabrication defects. Carrier concentrations of greater than about 1×10^{17} are preferred but the p^+ doping should be about an order of magnitude higher than the n^- doping. Suitable dopants for producing the p-type regions include aluminum, boron or gallium. Carrier concentrations of up to about 3×10^{17} cm^{-3} are suitable for the n^- epitaxial layers **20** and **21**, however, carrier concentrations of about 3×10^{16} or less are preferred. Suitable dopants for producing the n^- epitaxial layer include nitrogen and phosphorous. The optional n^+ epitaxial layer **15** is also preferably formed of n-type conductivity silicon carbide with carrier concentrations of greater than about 2×10^{16} and preferably greater than about 2×10^{18} cm^{-3}. Suitable dopants for producing the n^+ substrate and epitaxial layer include nitrogen or phosphorous. For the n^- regions of the diodes described above, including the substrate and epitaxial layers, carrier concentrations of about 5×10^{17} are suitable but carrier concentrations of about 1×10^{18} or higher are preferred.

The ohmic contacts **45**, and **46** are preferably formed of nickel or other suitable metals. The

Schottky contacts **40**, and **41** are preferably formed of platinum or platinum silicide, titanium or gold, however, other metals known to one skilled in the art to achieve the Schottky effect may be used.

Fabrication of devices according to the present invention begins with a starting material of a n^+ heavily doped silicon carbide bulk single crystal substrate. A lightly doped n^- epitaxial layer is then formed on the substrate through chemical vapor deposition. Optionally, the n^- layer is formed on an n^+ epitaxial layer which is also grown by chemical vapor deposition on a bulk single crystal silicon carbide substrate. Methods of forming such epitaxial layers are described in United States Patent No. 4,912,064, the disclosure of which is incorporated entirely herein by reference as if set forth fully.

After growth of the n^- epitaxial layer, a masked deep p-type implant is performed to define the p-type regions about the periphery of the anode or Schottky contact. Methods of forming a p-type implanted region are described in United States Patent No. 5,087,576, the disclosure of which is incorporated entirely herein by reference as if set forth fully.

The diode mesa is then formed by a masked etch which isolates adjacent devices and removes a portion of the p-type implanted region. The depth of the etching and the mask utilized depends upon the physical configuration of the particular device created. Furthermore, the depth of the trench is dependent upon whether the mesa is to be formed into the substrate or into the optional n^+ epitaxial layer as illustrated in **Figure 2**. Methods of etching such a mesa are known to those of skill in the art and include methods of reactive ion etching such as those described in United States Patent No. 4,981,551, the disclosure of which is incorporated herein by reference as if set forth fully.

Optionally, an insulating layer of SiO_2, Si_3N_4 or other various forms of glasses may be deposited or thermally grown over the entire top surface of the wafer including forming an insulating layer down the sidewalls of the mesa. Such an insulating layer may be formed by methods known to those of skill in this art, such as those described in United States Patent No. 5,459,107. Thicknesses of greater than about 500 angstroms are preferred and more preferably thicknesses of greater than 1 micron.

A cathode contact is formed on the back side of the substrate by forming an ohmic contact through the deposition and annealing of metal. Next, a masking step opens windows for the etching of the insulating layer and the subsequent deposition of Schottky metal. The mask opens windows such that the Schottky metal overlap of the p-type region of the device is minimized while maintaining overlap of the remaining upper surface of the mesa. The insulating layer is then wet etched and subsequently cleaned. Cleaning may be accomplished by a preclean of acetone, methanol and water for 5 minutes each followed by a hot HCL dip to remove surface metal contaminants. A water rinse and alkaline solution (such as $NH_4OH;H_2O_2$) will remove organic impurities. A Schottky metal is then deposited over the top of the entire wafer. The photo resist dissolving solution then lifts off the Schottky metal from areas where the Schottky metal was not deposited directly on a silicon carbide surface.

The present invention has been specifically described with respect to fabrication in silicon carbide which is the preferred embodiment of the present invention. However, as will be appreciated by those of skill in this art, the benefits of the present invention may be achieved through the use of other semiconductor materials such as silicon or gallium-arsenide. More particularly, the structure of the

present invention would provide benefits of increased reverse bias breakdown voltage and decreased leakage current if produced in other semiconductor materials than silicon carbide. However, the structures and methods of the present invention are particularly well suited to application in silicon carbide.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

THAT WHICH IS CLAIMED IS:

1. A Schottky barrier diode comprising:

a bulk single crystal substrate of n-type conductivity semiconductor material having a first surface and a second surface opposite said first surface;

an epitaxial layer of n-type conductivity semiconductor material formed on said first surface wherein said epitaxial layer has a lower carrier concentration than that of said substrate;

an ohmic contact formed on said second surface of said substrate opposite said epitaxial layer to provide a cathode contact;

a Schottky contact formed on said epitaxial layer to provide an anode contact wherein said Schottky contact has a periphery defined by the edges of said Schottky contact;

regions of p-type conductivity semiconductor material formed in said epitaxial layer wherein said regions are formed about the periphery of said Schottky contact and extend beneath said Schottky contact and past said edges of said Schottky contact while maintaining a region of contact between said n-type semiconductor material epitaxial layer and said Schottky contact; and

where said substrate and said epitaxial layer form a mesa having sidewalls which define the periphery of said diode, said sidewalls of said mesa extending downward through said regions of p-type conductivity semiconductor material and said epitaxial layer to said substrate.

2. The diode of claim 1 further comprising a insulating layer formed on the sidewalls of said mesa to passivated the sidewalls of said mesa.

3. The diode of claim 2 wherein said insulating layer also covers the portion of the upper surface of said p-type regions which extends past the edge of said Schottky contact.

4. The diode of claim 1 where said semiconductor material comprises silicon carbide.

5. The diode of claim 4 where said silicon carbide comprises 4H polytype silicon carbide.

6. A Schottky barrier diode comprising:

a bulk single crystal substrate of n-type conductivity silicon carbide having a first surface and a second surface opposite said first surface;

a first epitaxial layer of n-type conductivity silicon carbide formed on said first surface of said substrate;

a second epitaxial layer of n-type conductivity silicon carbide formed on said first epitaxial layer wherein said epitaxial layer has a lower carrier concentration than that of said first epitaxial layer substrate;

an ohmic contact formed on said second surface of said substrate opposite said first epitaxial layer to provide a cathode contact;

a Schottky contact formed on said second epitaxial layer to provide an anode contact wherein said Schottky contact has a periphery defined by the edges of said Schottky contact;

regions of p-type conductivity silicon carbide formed in said second epitaxial layer wherein said regions are formed about the periphery of said Schottky contact and extend beneath said Schottky contact and past said edges of said Schottky contact while maintaining a region of contact between said n-

type silicon carbide epitaxial layer and said Schottky contact;

where said second epitaxial layer forms a mesa having sidewalls which define the periphery of said diode, said sidewalls of said mesa extending downward through said regions of p-type conductivity silicon carbide and said second epitaxial layer to said first epitaxial layer.

7. The diode of claim 6 wherein said mesa is formed by said first and said second epitaxial layers and wherein said sidewalls of said mesa extend downward through said p-type conductivity regions and through said first and said second epitaxial layers to said substrate.

8. The diode of claim 6 further comprising a insulating layer formed on the sidewalls of said mesa.

9. The diode of claim 8 wherein said insulating layer also covers the portion of the upper surface of said p-type regions which extends past the edge of said Schottky contact.

10. The diode of claim 8 wherein said insulating layer is SiO_2.

11. The diode of claim 8 wherein said insulating layer has a thickness of about 1 micron.

12. The diode according to claim 6 wherein said silicon carbide comprises 4H polytype silicon carbide.

13. A method of reducing the leakage current and increasing the breakdown voltage of a Schottky barrier diode having a Schottky gate contact formed on

a lightly doped n-type conductivity epitaxial layer of semiconductor material, the method comprising;

forming p-type conductivity regions in the n-type epitaxial layer at the periphery of the Schottky contact of the diode;

etching through the p-type conductivity region and through the n-type conductivity epitaxial layer to form a mesa.

14. The method of claim 13 further comprising the step of forming an insulating layer on the sidewalls of the mesa formed by said etching step.

15. The method of claim 13 wherein the n-type conductivity epitaxial layer is formed on a first n-type epitaxial layer of higher carrier concentration and wherein said etching step comprises etching through the p-type conductivity regions and through the n-type conductivity epitaxial layer and through the first epitaxial layer to form a mesa.

16. The method of claim 13 further comprising the step of forming an insulating layer on the sidewalls of the mesa formed by said etching step.

17. The method according to claim 13 wherein the semiconductor material is silicon carbide.

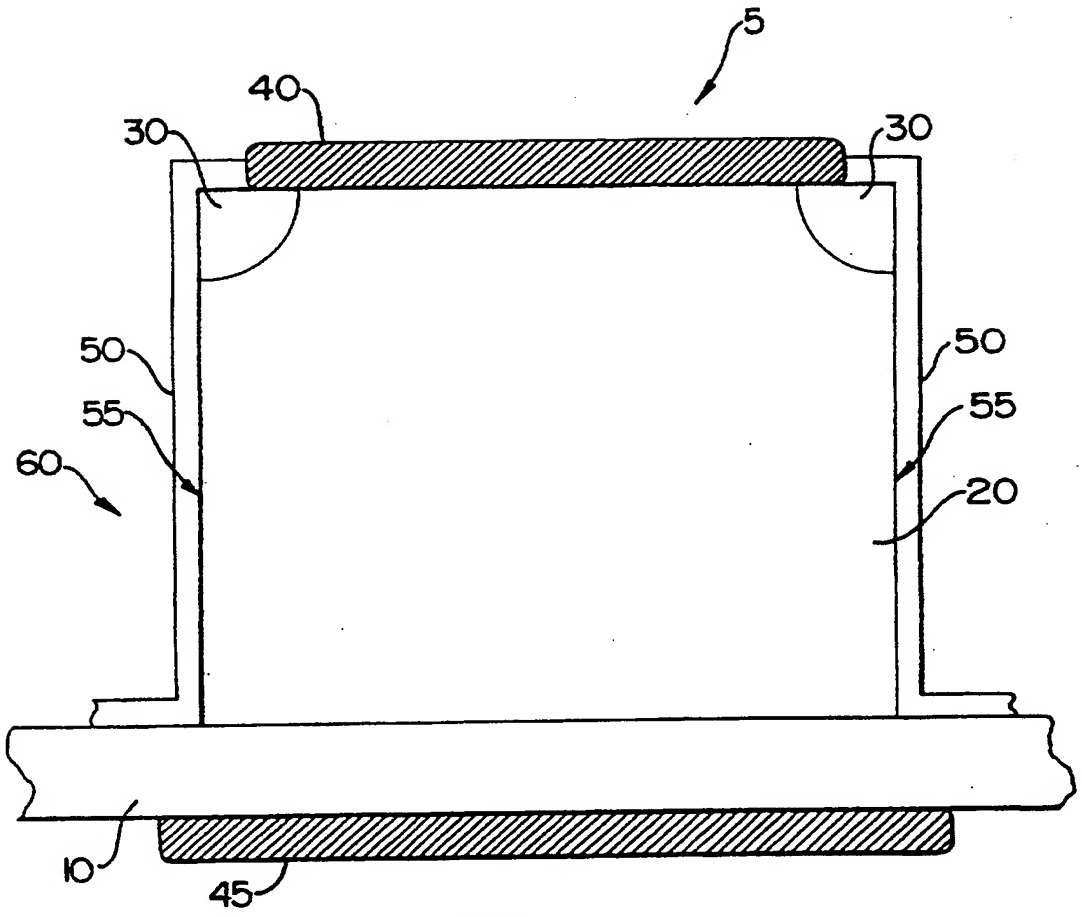

FIG. 1.

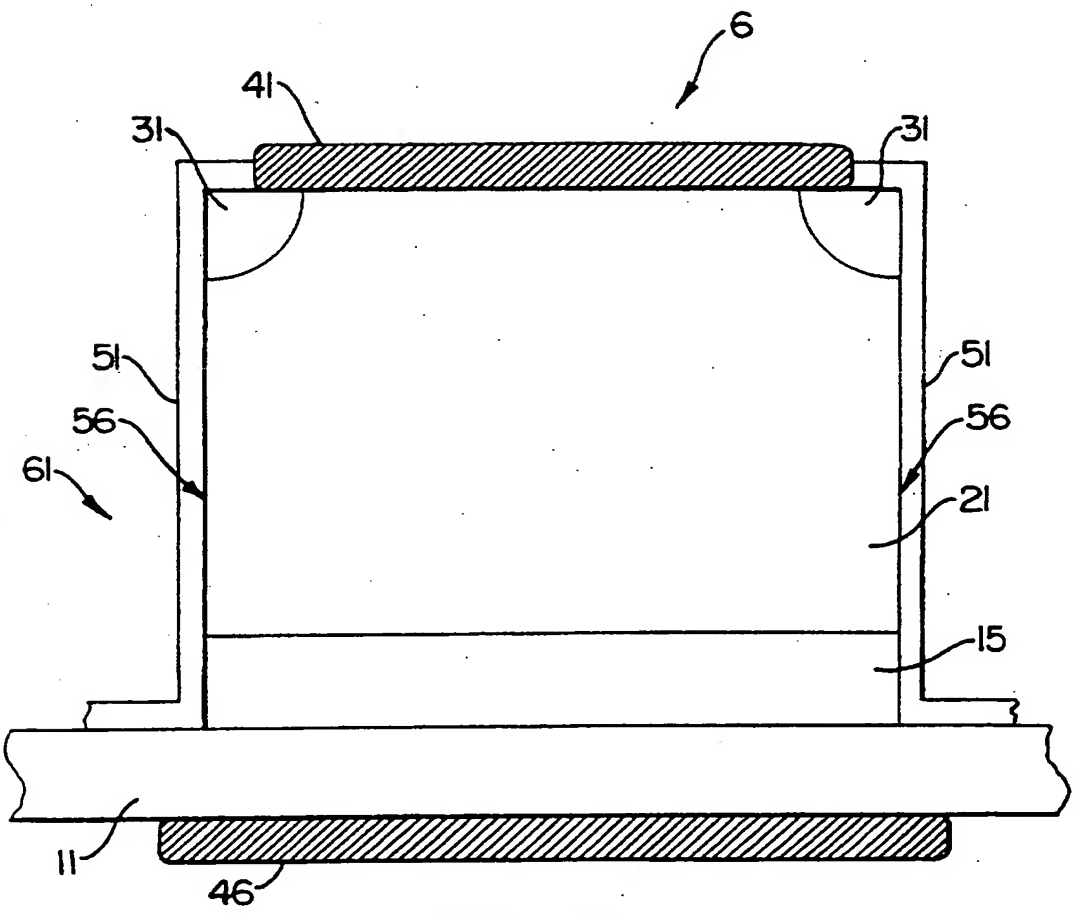

FIG. 2.

INTERNATIONAL SEARCH REPORT

Inten ial Application No
PCT/US 97/00335

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L29/06 H01L29/24 H01L21/04 H01L29/872

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	EP 0 093 866 A (SIEMENS AG) 16 November 1983 see figure 4	1-3,13, 14,16 4-12,15, 17

Y	SILICON CARBIDE AND RELATED MATERIALS 1995. PROCEEDINGS OF THE SIXTH INTERNATIONAL CONFERENCE, PROCEEDINGS OF INTERNATIONAL CONFERENCE ON SILICON CARBIDE AND RELATED MATERIALS, KYOTO, JAPAN, 18-21 SEPT. 1995, ISBN 0-7503-0335-2, 1996, BRISTOL, UK, IOP PUBLISHING, UK, pages 689-692, XP000652581 ITOH A ET AL: "Low power-loss 4H-SiC Schottky rectifiers with high blocking voltage" Page 690, "Experiments"	4-12,15, 17

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

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"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
19 March 1997	17.04.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Eliasson, G

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INTERNATIONAL SEARCH REPORT

Inte. ɔnal Application No
PCT/US 97/00335

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	IEEE ELECTRON DEVICE LETTERS, vol. 17, no. 3, 1 March 1996, pages 139-141, XP000584756 ITOH A ET AL: "EXCELLENT REVERSE BLOCKING CHARACTERISTICS OF HIGH-VOLTAGE 4H-SIC SCHOTTKY RECTIFIERS WITH BORON-IMPLANTED EDGE TERMINATION" see the whole document ---	1-17
X	US 4 720 734 A (AMEMIYA YOSHIHITO ET AL) 19 January 1988 see column 7, line 33-52; figure 6 ---	1-3,13, 14,16
A	EP 0 380 340 A (CREE RESEARCH INC) 1 August 1990 see abstract -----	1-17

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